REMARKS

Claim 1-31 remain pending in the application. Reconsideration is respectfully requested in light of the following remarks.

Section 103(a) Rejection:

The Examiner rejected claims 1-31 under 35 U.S.C. § 103(a) as being unpatentable over Lynch et al. (U.S. Patent 5,938,748) (hereinafter "Lynch"). Applicants respectfully traverse this rejection for at least the following reasons.

Lynch fails to teach or suggest all of the limitations of Applicants' claim 1. Specifically, Lynch fails to teach or suggest a system comprising data capture logic configured to capture data events from a nondeterministic data bus; a system memory including a plurality of addressable locations, wherein a subset of the plurality of addressable locations is configured as a data event buffer; a direct memory access (DMA) transfer engine coupled to the data capture logic and to the system memory and configured to perform a DMA transfer operation of the captured data events from the data capture logic to a region of the data event buffer as portions of the captured data events become available from the data capture logic; and an application configured to access the data event buffer to process the captured data events without the DMA transfer operation being stopped; wherein in response to the region of the data event buffer being filled, the DMA transfer engine is further configured to perform the DMA transfer operation to a different region of the data event buffer without the DMA transfer operation being stopped.

First, Lynch fails to teach or suggest logic configured to capture data events from a nondeterministic data bus. Lynch is instead directed to transferring communications traffic via a synchronous, real-time serial bus (col. 4, line 31 – col. 5, line 7; col. 6, lines 23-42). By definition, such a bus is deterministic, not nondeterministic. In FIG. 2, Lynch clearly illustrates transmit and receive portions of the

serial interface that is the object of Lynch's disclosure as including a clock signal (CLK). Throughout his disclosure, Lynch characterizes the operation of transmitting and receiving serial data as a clock-synchronous, streaming operation. But by their nature, clock-synchronous operations are deterministic operations, not non-deterministic operations. That is, the presence of a bus clock coordinates and defines precise timeframes in which data events and their capture may occur. Valid data transfer may only occur at proper times as determined by the state of the bus clock. While Lynch describes various modes in which data *packets* may be transmitted synchronously or asynchronously, the individual data *events* that occur on the data bus in order to transmit a packet are, in Lynch, universally clock-synchronous. Lynch does not disclose a non-deterministic bus.

Second, Lynch does not disclose performing a DMA transfer operation of data events captured from a nondeterministic data bus to a region of a data event buffer as portions of the captured data events become available from the data capture logic, wherein in response to the region of the data event buffer being filled, the DMA transfer engine is further configured to perform the DMA transfer operation to a different region of the data event buffer without the DMA transfer operation being stopped. The Examiner relies on col. 2, line 45 – col. 3, line 39 and col. 7, lines 27-51 to support these limitations of claim 1. Applicants can find no language having anything to do with DMA transfer of captured data events into a data event buffer as recited in claim 1 within the first cited passage, which discusses synchronous transmission of data via a serial bus. In fact, this passage mentions the contemplated *elimination* of DMA and data buffering from Lynch's telecommunications device.

Regarding col. 7, lines 27-51 and FIG. 4, Lynch clearly describes circular buffer 20 as being used to buffer frames of data that are to be *transmitted via* Lynch's synchronous serial link, not data events *captured from* a nondeterministic data bus. Specifically, this passage specifies that "... data to be transmitted to the telecommunications device be at least double buffered." Each entry of buffer 20 "holds one DSP frame of data" – that is, data that is produced by the DSP for transmission, not

data events captured from a nondeterministic data bus for further processing by an application. Lines 40-51 of Lynch are unambiguous in specifying that buffer 20 operates to receive data from the DSP for transmission via the telecommunications devices, which is precisely the opposite of the mode of operation of claim 1. Claim 1 is directed to the DMA transfer of data events that have been captured from a nondeterministic data bus into one region of a data event buffer that may continue into a different region when the first region is filled without stopping the DMA transfer. Lynch makes no mention whatsoever of these aspects of buffering received, captured data events.

For at least the reasons given above, Applicants submit that the rejection of independent claim 1 is clearly unsupported by the cited art, as is the rejection of independent claims 11 and 22 which recite limitations similar to those of claim 1.

With reference to claims 5, 16 and 26, the Examiner asserts that although Lynch fails to disclose the limitation where a nondeterministic data bus conforms to the IEEE-488 GPIB standard, "[n]onetheless, one of ordinary skill would readily recognize that the IEEE-488 GPIB standard is well known in the art, thereby making use of this type of bus obvious to one of ordinary skill." Applicants traverse the Examiner's statements.

As argued with respect to similar rejections raised in the previous Office Action, these features may be well known in other contexts. However, as the Federal Circuit stated in *In re Kotzab*, 55 USPQ2d 1313, 1316 (Fed. Cir. 2000):

> Most if not all inventions arise from a combination of old elements. However, identification in the prior art of each individual part claimed is insufficient to defeat patentability of the whole claimed invention. Rather, to establish obviousness based on a combination of the elements disclosed in the prior art, there must be some motivation, suggestion or teaching of the desirability of making the specific combination that was made by the applicant. (emphasis added)

Thus, the Examiner's assertion that circular and linear data event buffers as well as the IEEE-488 bus are well known does not establish that the prior art teaches Applicants' specifically claimed application of these elements in combination with the other claimed elements. The evidence of record does not indicate the desirability of circular and linear

data event buffers or the IEEE-488 bus as combined in Applicants' claims. Moreover, as the Court of Appeals for the Federal Circuit recently explained in *In re Sang Su Lee*, Docket No. 00-1158 (Fed. Cir. January 18, 2002), conclusory statements such as those provided by the Examiner that a claim limitation is well known or common knowledge do not fulfill the Examiner's obligation. "Deficiencies of the cited references cannot be remedied by the [Examiner's] general conclusions about what is 'basic knowledge' or 'common sense.'" *In re Zurko*, 59 USPQ2d 1693, 1697 (Fed. Cir. 2001). "Common knowledge and common sense ... do not substitute for authority." *In re Sang Su Lee.* Common knowledge "does not in and of itself make it so" absent evidence of such knowledge. *Smiths Industries Medical Systems, Inc. v. Vital Signs, Inc.*, 51 USPQ2d 1415, 1421 (Fed. Cir. 1999). Thus, Applicants submit that the rejection of these claims is improper.

With reference to claims 8, 19 and 29, the Examiner acknowledges that Lynch does not disclose that processed data events are displayed substantially in real time with respect to the occurrence of the corresponding captured data events on a nondeterministic data bus, but asserts that "Lynch does teach real-time monitoring by network administrators via host computer 100. Therefore, one of ordinary skill would readily recognize that some sort of display means could be used during the monitoring process." Applicants traverse the Examiner's statements. Applicants note that the referenced claims do not in fact recite "some sort of display means," but in fact recite a specific manner of display that the Examiner has acknowledged is absent from the art of record. As noted in the previous paragraph, Applicants submit that actual evidence and not mere speculation as to the existence of these features in the prior art is required. Absent such evidence, Applicants submit that no *prima facie* case of obviousness has been established with respect to these claims.

Applicants further note that numerous ones of the dependent claims recite additional features not taught or suggested by any of the cited references taken individually or in any combination. However, as the rejection of the independent claims

has been shown to be unsupported by the cited art, no further discussion of the dependent claims is necessary at this time.

CONCLUSION

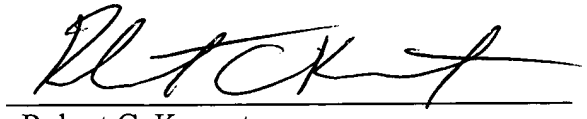
Applicants submit the application is in condition for allowance, and prompt notice to that effect is respectfully requested.

If any extension of time (under 37 C.F.R. § 1.136) is necessary to prevent the above-referenced application from becoming abandoned, Applicants hereby petition for such an extension. If any fees are due, the Commissioner is authorized to charge said fees to Meyertons, Hood, Kivlin, Kowert, & Goetzel, P.C. Deposit Account No. 501505/5150-83700/RCK.

Also enclosed herewith are the following items:

- ☒ Return Receipt Postcard
- ☐ Petition for Extension of Time
- ☐ Notice of Change of Address
- ☐ Other:

Respectfully submitted,



Robert C. Kowert
Reg. No. 39,255
ATTORNEY FOR APPLICANT(S)

Meyertons, Hood, Kivlin, Kowert, & Goetzel, P.C.
P.O. Box 398
Austin, TX 78767-0398
Phone: (512) 853-8850

Date: November 2, 2006